

## Claims

1. An integrated read-only memory, comprising  
a plurality of selection transistors each having a drain connection,  
an electrode for feeding a voltage or a current;  
5 a layer between each drain connection and the electrode, having a  
modifiable electrical resistance through a configuration electrical signal,  
a source connection per selection transistor;  
a bit line that is electrically connected to at least one source connection;  
where the layer is formed as a common layer for linking the drain  
10 connections to the electrode, and where the electrical resistance of the layer can  
be changed locally.
2. The read-only memory of claim 1, where the resistance of the layer can  
be switched over.
3. The read-only memory of claim 1 where the resistance of the layer can  
15 be switched over between multiple resistance characteristic curves.
4. The read-only memory of claim 1, comprising:  
a read signal applied to the layer within a defined signal range in a read  
operation of the read-only memory, and  
a configuration signal outside the read signal range in a configuration  
20 operation of the read-only memory.
5. The read-only memory of claim 1, where the read-only memory is a  
flash memory.
6. The read-only memory of claim 1, where the selection transistors are  
arranged in an array.
- 25 7. The read-only memory of claim 1, where the bit line is connected to a  
decoder circuit.
8. The read-only memory of claim 1, where the bit line is accessible for an  
external connection.

9. The read-only memory of claim 1, comprising:  
a gate connection per selection transistor; and  
a word line being electrically connected to at least one gate connection.
10. The read-only of claim 9, where the word line is connected to a decoder  
5 circuit.
11. The read-only memory of claim 9, where the word line is accessible for  
an external connection.
12. The read-only memory of claim 9, where the selection transistors have a  
substantially planar construction in the substrate.
- 10 13. The read-only memory of claim 1, where the selection transistors have a  
vertical construction in the substrate.
14. The read-only memory of claim 1, where the layer is formed as a  
molecular layer.
15. The read-only memory of claim 14, where the layer contains rotaxane.
- 15 16. The read-only memory of claim 14, where the layer contains catenane.
17. The read-only memory of claim 14, where the layer contains a  
bispyridinium compound.
18. The read-only memory of claim 1, where the layer is formed as a  
dielectric.
- 20 19. The read-only memory of claim 18, where the layer contains  $\text{SrZrO}_3$ .
20. The read-only memory of claim 1, where the layer is formed as a  
polymer.
21. The read-only memory of claim 20, where the layer contains 3-  
nitrobenzal malonitrile, 1,4-phenylenediamine complex.

22. The read-only memory of claim 20, where the layer contains a chalcogenide compound.

23. A method for operating an integrated read-only memory having a plurality of selection transistors each having a drain connection and an electrode for feeding a voltage or a current, including a layer between each  
5 drain connection and the electrode,, comprising:

providing a layer between each drain connection and the electrode, the layer having a modifiable electrical resistance through a configuration electrical signal, where the layer is formed as a common layer for linking the drain  
10 connections to the electrode, and where the electrical resistance of the layer can be changed locally; applying in a read operation, a read voltage or a read current within a defined voltage or current range is applied to the layer; and

applying in a configuration operation, a configuration voltage or a configuration current outside the voltage or current range provided for the read  
15 operation is applied to the layer.

24. A method for producing an integrated read-only memory, comprising:

producing an array of selection transistors using CMOS technology;

leading drain contacts of the selection transistors to the surface of the arrangement;

20 depositing a layer having an electrical resistance that can be changed through the effect of a configuration signal, where the electrical resistance of the layer may be changed locally;

arranging an electrode is arranged above the layer;

forming a source connection per selection transistor;

25 forming a bit line which is electrically connected to at least one source connection; and

forming the layer as a common layer for linking the drain connections to the electrode.

25. The method for producing an integrated read-only memory of claim 24,  
30 where the layer is deposited as a common layer for linking the drain connections to the electrode above the selection transistors.

26. The method for producing an integrated read-only memory of claim 24, where the selection transistors are produced in a front end process.
27. The method for producing an integrated read-only memory of claim 24, where the layer is deposited in a back end process.
- 5 28. The method for producing an integrated read-only memory of claim 24, where the selection transistors are constructed in substantially planar fashion in the substrate.
29. The method for producing an integrated read-only memory of claim 24, where the selection transistors are constructed vertically in the substrate.
- 10 30. The method for producing an integrated read-only memory of claim 24, where the layer is formed as a molecular layer.
31. The method for producing an integrated read-only memory of claim 30, where the layer contains rotaxane.
32. The method for producing an integrated read-only memory of claim 30,  
15 where the layer contains catenane.
33. The method for producing an integrated read-only memory of claim 30, where the layer contains a bispyridinium compound.
34. The method for producing an integrated read-only memory of claim 24, where the layer is formed as a dielectric.
- 20 35. The method for producing an integrated read-only memory of claim 34, where the layer contains  $\text{SrZrO}_3$ .
36. The method for producing an integrated read-only memory of claims 24, where the layer is formed as a polymer.
37. The method for producing an integrated read-only memory of claim 36,  
25 where the layer contains a 3-nitrobenzal malonitrile, 1,4-phenylenediamine complex.

38. The method for producing an integrated read-only memory of claims 24, where the layer contains a chalcogenide compound.